INtelligent, **F**ast, **I**nterconnected and **E**fficient devices, for frontier exploitation in **R**esearch and **I**ndustry
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NATURE OF THE DELIVERABLE: ☐**R**= Report
BENEFICIARY(IES) CONTRIBUTOR(S): INFN, CERN, FNAL, RAL/UBRIS, STFC, CNRS

AUTHOR(S) NAME(S) & EMAIL(S):
Giacomo Fedi (ER1), Giacomo.Fedi@pi.infn.it
Fabrizio Palla, Fabrizio.Palla@pi.infn.it
Guido Magazzù, Guido.Magazzu@pi.infn.it
Ian Tomalin, ian.tomalin@stfc.ac.uk
Claire Shepherd-Themistocleous, Claire.Shepherd-Themistocleous@cern.ch
Dave Newbold, Dave.Newbold@cern.ch
Davide Cieri (ESR11), Davide.Cieri@stfc.ac.uk
Luigi Calligaris (ER2), Luigi.Calligaris@stfc.ac.uk
Luis Ardila-Perez (ER11.2), Luis.Ardila@stfc.ac.uk
Ted Liu, Thliu@fnal.gov

Abstract

To profit from the High Luminosity run of the LHC collider, which is foreseen to start in ~2025, major upgrades are required to the LHC detectors. In particular, the CMS experiment must improve its level-1 trigger system, whose purpose is to rapidly identify interesting collision events. To make this possible, CMS must reconstruct the trajectories of charged particles recorded within its tracking detector within ~4 μs. This is an exceptionally challenging project, which is being undertaken within the context of INFERI. A few alternative solutions to the problem are being explored, notably one named "TMTT", which uses FPGAs and is developed by STFC, CERN, KIT & Vienna; and another using custom `associative memory' (AM) chips in combination with FPGAs, developed by the INFN, FNAL, KIT, CNRS, Kolkata and several other US and Brasilian universities

The track reconstruction algorithms have been developed and optimized using C++ software running on simulated LHC collision data. The chosen algorithms were then written in VHDL for loading onto FPGA with and without the usage of dedicated AM chips.

In the case of the TMTT solution, the software studies established that track-finding in the plane perpendicular to the beam-line using a technique known as a Hough Transform provided quick, preliminary track reconstruction with an algorithm simple enough to be loaded into an FPGA. These tracks were then cleaned up and fitted using

either a Kalman Filter track fit, or an alternative solution based on cleaning the tracks in a plane containing the beam-line (with an algorithm known as a Seed Filter) followed by a simple Linear Regression track fit. Finally, a Duplicate Removal algorithm is run to eliminate particles that were accidentally reconstructed twice.

INFIERI researcher D.Cieri (ESR11) was responsible for the Seed Filter, doing both the software studies and the VHDL implementation. He also played an important role in improving the Linear Regression fitter (again with both software and VHDL). L.Calligaris (ER2) performed software studies of the Duplicate Removal algorithm and Luis Ardila-Perez (ESR11.2) implemented it in VHDL.

In the case of the AM solution the pattern recognition is performed in the AM chips, where the hit positions are matched to preloaded coarse-resolution tracks (aka patterns). About 0.5 patterns are needed to give fully efficient pattern recognition with fake rates of the order of ~15% for ttbar events in 200 pileup collisions. The stubs in the matched patterns are then filtered in the FPGA with some combinatorial algorithms and then fitted in the FPGA with fast algorithms based on principal component analysis. The final step in the FPGA removes duplicate tracks that share several stubs.

The tracking performance obtained with these algorithms is shown in the report for Deliverable 4.11.

Publications

N.B. Many of the publications listed here were also presented at conferences. Only publications related to the L1 tracking work are listed here, but the INFIERI fellows are also on the author list of numerous other CMS papers.

- G. Fedi, et al. "A pattern recognition mezzanine based on associative memory and FPGA technology for L1 track triggering at HL-LHC", poster presented by G. Fedi at "Frontier Detectors for Frontier Physics", La Biodola (Isola d'Elba, Italy), 24-30 May 2015, published in Nuclear Instruments & Methods in Physics Research A (2015), http://dx.doi.org/10.1016/j.nima.2015.09.086
- G. Fedi et al, "A Pattern Recognition Mezzanine based on Associative Memory and FPGA technology for Level 1 Track Triggers for the HL-LHC upgrade", presented by D. Magalotti at "TWEPP2015", Lisbon (Portugal), 28 Sept. – 2 Oct. 2015, to be published in JINST.
- F. Palla, M. Pesaresi and A. Ryd, "Track Finding in CMS for the Level-1 Trigger at the HL-LHC", presented by M. Pesaresi at "TWEPP2015", Lisbon (Portugal), 28 Sept. – 2 Oct. 2015, **JINST 11 (2016) no.03, C03011,**
- http://dx.doi.org/10.1088/1748-0221/11/03/C03011
- D. Cieri *et al.*, " L1 track finding for a time multiplexed trigger, Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment", ISSN 0168-9002, http://dx.doi.org/10.1016/j.nima.2015.09.117.
- D. Cieri *et al.*, "Hardware Demonstrator of a Level-1 Track Finding Algorithm with FPGAs for the Phase II CMS experiment", proceedings from the ACAT2016 conference, IOP Publishing, Journal of Physics: Conference Series 762 (2016) 012020, doi:10.1088/1742-6596/762/1/012020C.
- **G. Fedi, G. Magazzù, F. Palla.** et al, Track finding based on Associative Memories for Level-1 Triggering in HL-LHC experiments, best paper to the MOCAST 2016 conference, Thessaloniki, Greece, 12-14 May 2016, https://doi.org/10.1109/MOCAST.2016.7495145

- D.Cieri, L.Calligaris *et al.*, "An FPGA-based track finder at Level-1 for the CMS experiment at the High Luminosity LHC", proceedings for the 2016 IEEE Real Time Conference, doi:10.1109/RTC.2016.7543102
- D.Cieri, L.Calligaris *et al.*, "Emulation of a prototype FPGA track finder for the CMS Phase-2 upgrade with the CIDAF emulation framework", proceedings for the 2016 IEEE Real Time Conference, DOI: 10.1109/RTC. 2016.7543110
- D.Cieri, L.Calligaris, L.Ardila-Perez *et al., a comprehensive paper on the FPGA-based track-finding solution is in preparation for publication in JINST.*
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- G. Fedi G., A Pattern Recognition Mezzanine Based on Associative Memory and FPGA Technology for Level-1 Track Triggers for the HL-LHC Upgrade", 2015 IEEE Nuclear Science Symposium and Medical Imaging Conference, San Diego, USA 31Oct-7 Nov, 2015
- G.Fedi ``Associative Memory Pattern Matching for the L1 Track Trigger of CMS at the HL-LHC,'' EPJ Web Conf. 127 (2016) 00008. doi:10.1051/epjconf/201612700008, Connecting the Dots 2016, 22-24 Feb 2016 Vienna (Austria)
- G. Fedi, L1 track trigger for the CMS HL-LHC upgrade using AM chips + FPGA" , CDT/ WIT 2017, Orsay, France 6-9 March, 2017

Talks (not counting those listed under Publications)

All INFIERI fellows on this project have given numerous talks at internal CMS meetings. In addition, they have given the following talks at conferences:

- G. Fedi et al., "A Pattern Recognition Mezzanine based on Associative Memory and FPGA technology for Level-1 Track Triggers for the HL-LHC Upgrade", presented by G. Fedi at "2015 IEEE Nuclear Science Symposium & Medical Imaging Conference", San Diego (USA), 31 Oct. – 7 Nov. 2015.
- G. Fedi, "The L1 Track Finder based on Associative Memories", Talk at the "Vth INFIERI workshop", CERN, Geneva (Switzerland), 27-29 April 2015, https://indico.cern.ch/event/381514/session/6/contribution/13/2/attachments/760406/1043083/infieri.pdf
- 6th INFIERI Workshop, Pisa, Italy 27-29 October, 2015 Talk contribution: "Latest on A.M. based Track Finder" Talk contribution: "Status for A.M. based integration test bench for A.M. based L1 track finder"
- D. Cieri, "The L1 Track Finder based on an all-FPGA's architecture", Talk at the "Vth INFIERI workshop", CERN, Geneva (Switzerland), 27-29 April 2015, https://indico.cern.ch/event/381514/session/6/contribution/13/0/attachments/1132267/1618793/Infieri-workshop.pdf
- D. Cieri, "Track Finding Algorithm for the L1 Track Trigger of the Phase II CMS Experiment", at the IVth INFIERI Workshop – Amsterdam 10-12 December, 2014, https://indico.cern.ch/event/352552/contribution/16/material/slides/4.pdf
- D.Cieri, "L1 Track Finding for a time multiplexed trigger", at the 13th Pisa Meeting on Advanced Detectors, La Biodola, Isola D'Elba, Italy, 24-30 May 2015,

https://agenda.infn.it/getFile.py/access?contribId=421&sessionId=17&resId=0&materialId=poster&confId=8397

- D.Cieri, "L1 Track Finding for a time multiplexed trigger", at the Postgraduate days, University of Bristol, Bristol, 15 June 2015
- D.Cieri, "Hardware Demonstrator of a L1 Track Finding Algorithm with FPGAs for the Phase II CMS Experiment", to be presented at the 17th International workshop on Advanced Computing and Analysis Techniques in physics research (ACAT), 18-22 January 2016, Valparaiso, Chile
- L.Calligaris, "Circuit Data Flow (CIDAF): A generic, flexible, discrete-time simulator", 3rd International Summer School on INtelligent Signal Processing for FrontIEr Research and Industry, Hamburg, 14-25 Sept 2015, https://indico.desy.de/conferenceOtherViews.py?view=standard&confId=12535
- L.Calligaris, "Trigger level track reconstruction in CMS with a fully time-multiplexed architecture using a Hough transform implemented in an FPGA", PoS(ICHEP2016)1000
- 7th INFIERI Workshop, Lisbon, Portugal 12-15 April, 2016 Talk contribution: "Progress report on AM at INFN-Pisa""
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- L.Calligaris, "Development of a multi-purpose circuit data flow simulation framework" , 6th INFIERI Workshop, Pisa, 28 Oct 2015, https://indico.cern.ch/event/404880/
- L.Calligaris, "The Track Trigger Proposal, An FPGA-based Level1 track trigger for the Phase-2 CMS Upgrade",
  UK CMS Annual Meeting, 14-15 Jan 2016, Brunel University London

Poster Presentations (not counting those listed under Publications)

- D.Cieri, L.Calligaris "Demonstrator Plans for FPGA-based L1 Track-finding with Hough Transform", at the 3rd International School on Intelligent Signal Processing for Frontier Research & Industry, 14-25 September 2015, Hamburg, Germany, http://infieri-network.eu/sites/default/files/Infieri-poster-hamburg-DCieri.pdf

Outreach

L.Calligaris and D.Cieri both participated in the annual STFC RAL master classes on experimental particle physics for hundreds of high school students.

G. Fedi Poster "PhaseII upgrades @CMS" - Researchers' Night, Pisa, Italy, September 25, 2015

G. Fedi Staff member - Bright Pisa - Researchers' Night, Pisa, Italy , September 30, 2016

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