INtelligent, **F**ast, **I**nterconnected and **E**fficient devices, for frontier exploitation in **R**esearch and **I**ndustry
Funding Scheme: FP7-PEOPLE-2012-ITN
Grant Agreement number: 317446
Project acronym: INFIERI

DELIVERABLE NAME: ***Development of the prototype VHDL design and algorithms for the High Level Processing Prototype for Positron Emission Tomography.***
DELIVERABLE REF. N°: 4.5
WORK PACKAGE: WP4
NATURE OF THE DELIVERABLE: ☒**R**= Report, ☒**P** = Prototype
BENEFICIARY(IES) CONTRIBUTOR(S): UC3M
AUTHOR(S) NAME(S) & EMAIL(S): Rigoberto Chil (rchil@hggm.es), Georgios Konstantinou (gkonstantinou@hggm.es), Juan Jose Vaquero (jjvaquer@ing.uc3m.es)
DELIVERY DATE FROM ANNEX 1: 36
DISSEMINATION LEVEL: ☒**RE**, ☐**CO**
PU = Public N/A IN THE INFIERI CONTEXT
PP = Restricted to other programme participants (including the Commission Services) N/A IN THE INFIERI CONTEXT
RE = Restricted to a group specified by the consortium (including the Commission Services) **HIGHLY SUGGESTED IN THE INFIERI CONTEXT**
CO = Confidential, only for members of the consortium (including the Commission Services) **HIGHLY SUGGESTED IN THE INFIERI CONTEXT**

Abstract:

The High level processing VHDL design and related algorithms have been developed for the application of novel hybrid FPGAs in the readout of a PET detector demonstrator.

For the initial prototype, comprising mainly of a Texas Instruments ADS6425 connected to a Xilinx Zinq7020 (figure 1), it was required to build some basic firmware, to allow for the digital information to be pipelined and transmitted to a central processing unit. In our case, applying the advantages provided by the hybrid programmable logic/microprocessor character of the Xilinx Zinq family, we proceeded with building a basic outline for the manipulation of the data received from the ADC.

As demonstrated in figure 2, the 4 ADC inputs that arrive at a maximum rate of 125MHz per word, are received at the programmable logic part, where after deserialization they are stamped for channel origin. The new words are then pipelined through FIFOs to a central multiplexing unit. From this unit data are being directed through a central FIFO towards the microprocessor

part of the Zinq, where a basic bare metal program ensures the correct transmission towards a PC, through USB serial protocol.

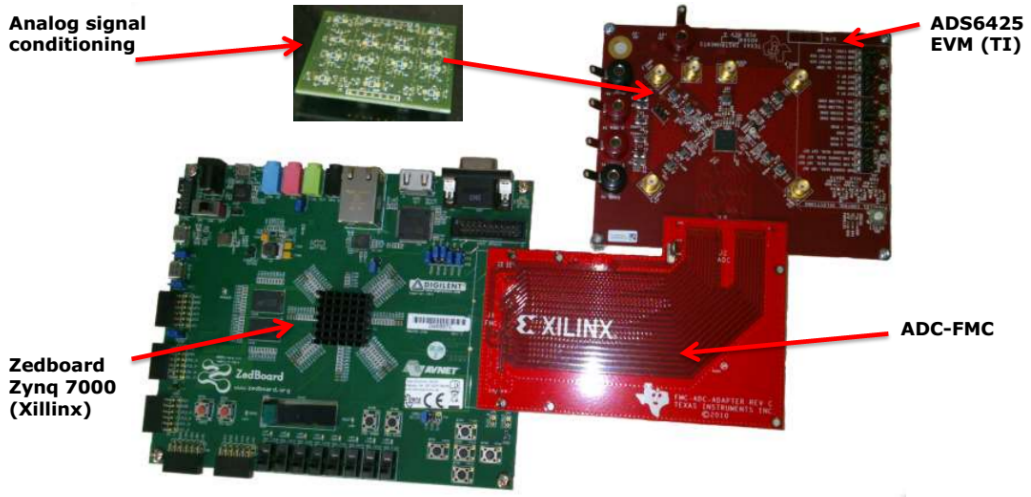

Figure 1: System prototype for the integration of an ADC and FPGA for the readout of SiPM based detectors

This basic architecture covers the main aspects necessary for the backbone of a data acquisition system, while furthermore allowing the application of higher level preprocessing algorithms on the raw data, such as triggering and event matching in the programmable part, as well as further communication and processing possibilities in the microprocessor, which is big enough to even accommodate a full lightweight linux distribution, such as RPi, Archlinux or the dedicated Xilinux.

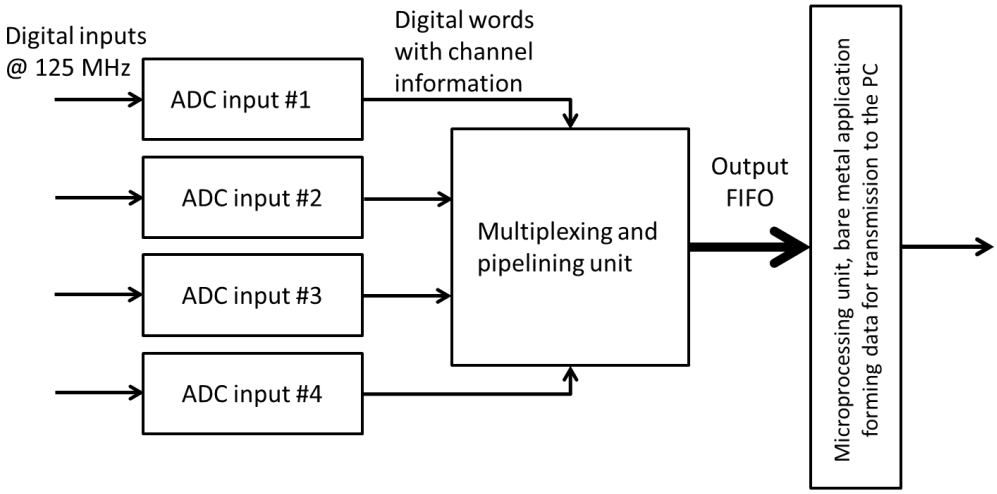

Figure 2: FPGA architecture