**INtelligent, Fast, Interconnected and Efficient devices, for frontier exploitation in Research and Industry**
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**Project acronym: INFIERI**


**DELIVERABLE NAME:** ***Prototype design, evaluation & tests results of a Level 1 trigger (real time selection) system for Proton Emission Tomography (PET)***
**DELIVERABLE REF. N°: 1.13**
**WORK PACKAGE: WP1**
**NATURE OF THE DELIVERABLE:** ☐**R**= Report, ☒**P** = Prototype
**BENEFICIARY(IES) CONTRIBUTOR(S): UC3M**
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**DISSEMINATION LEVEL:** ☒**RE,** ☐**CO**

**PU** = Public N/A IN THE INFIERI CONTEXT
**PP** = Restricted to other programme participants (including the Commission Services) N/A IN THE INFIERI CONTEXT
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## Abstract:

The level-1 trigger (i.e. real time selection) electronics system has been developed for a miniature spectrometer for nuclear medicine applications to PET-MRI.

### Work description:

Following the research already conducted in the University Carlos III of Madrid (UC3M), a special effort has been put into the development of a new readout system. The current design uses as controlling unit with a USB interface to the computer. The new design will have to take into consideration the special limitations introduced by the need of electronics miniaturization and MRI compatibility.

*The main features of this system is based on an FPGA to control a fast (>50 MHz) ADC, for digital pulse processing*

Indeed, as an innovative possibility, different from the standard analog pulse integration that has been used in previous developments, it is also worth considering the use of novel fast ADCs, that will allow directly sampling the analog pulse coming from the detector. In this case the raw output of the ADCs will account to very large amounts of data, so the use of an FPGA as a control unit, to trigger and compress the data, is mandatory. To investigate this solution, in which neither delay nor integration stages would be necessary, we used a Texas Instruments ADS6425 connected to a Xilinx Zinq7020. For this purpose, the development of three different boards were requested, one for the ADC, one Zedboard including the Zynq FPGA and a third board to connect the two of them. The innovative design of this FPGA, which apart from the programmable logic also includes two ARM microprocessor cores, provides a good solution for the development of a standalone system that appart from the firmware preprocessing can be loaded with software for data timing and network distribution. The programmable logic part is programmed using the common VHDL language so it can be easily replicated to include multiple ADCs using the same FPGA, and also be used on other systems with a similar architecture. This work is also on the prototyping level, but it has produced interesting results, especially on the case of a hand-held gamma camera.

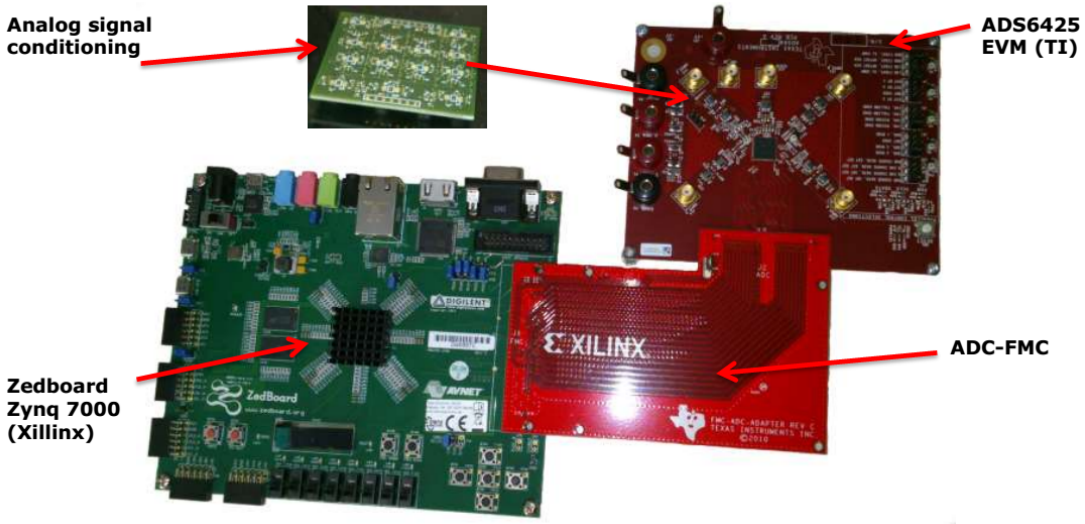


**Figure 1: System prototype for the integration of an ADC and FPGA for the readout of SiPM based detectors**

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**Dissemination:**

This work has been partly presented at the INFIERI summer school in July 2014 as a poster, named "**Development of a compact gamma camera for intra operative radiation imaging** ", by Konstantinou G., Chil R., Desco M., and Vaquero J.J.

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