INtelligent, **F**ast, **I**nterconnected and **E**fficient devices, for frontier exploitation in **R**esearch and **I**ndustry

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DISSEMINATION LEVEL: ☒**RE**, ☐**CO**

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Abstract

This deliverable builds on those described in the reports for Deliverables 4.9 and 4.10, which should be read first. It explains how hardware demonstrator systems were exploited, which were constructed to prove that the proposals for reconstructing charged particle tracks within ~4 μs at the upgraded CMS detector are viable. Two such proposals are being pursued within the context of INFIERI. The first, named "TMTT", uses FPGAs and is developed by STFC, CERN, KIT & Vienna. The second uses custom `associative memory' (AM) chips in combination with FPGAs, developed by INFN, FNAL, KIT, CNRS, Kolkata and several other US and Brasilian universities. .

1) **In the case of the TMTT solution**, the hardware demonstrator consisted of a number of high-speed data processing cards, known as MP7's, each equipped with a Xilinx Virtex7 FPGA. Track reconstruction algorithms

(known as the "TFP") were loaded onto the FPGAs, and were capable of reconstructing the tracks in one eighth of the tracker solid angle for one event in 36. Tracker stub data from simulated LHC collision events taken with up to 200 pile-up were injected into the TFP via additional MP7's that acted as a data source. Tracks reconstructed by the TFP were written to a further MP7, used as a data sink, from where they were read out. Comparison software, written by Davide Cieri (ESR11) compared these reconstructed tracks with those predicted by an implementation of the TFP algorithms in software. Excellent agreement was seen. For very detailed studies, the tracks reconstructed by the demonstrator were also compared with a full software emulation of the algorithms, capable of predicting the clock cycle in which each reconstructed track would appear. This emulation was written by Luigi Calligaris (ER2). These two INFIERI fellows, together with Luis Ardila-Perez (ESR11.2) used the demonstrator to debug the TFP and measure its performance. A typical result is the measurement of the tracking efficiency shown in Fig. 1. Excellent efficiency and helix parameter resolution are obtained, with good agreement between hardware and emulation. The time required for the TFP to reconstruct the tracks is 3.8 μs, which is fast enough to meet CMS requirements.

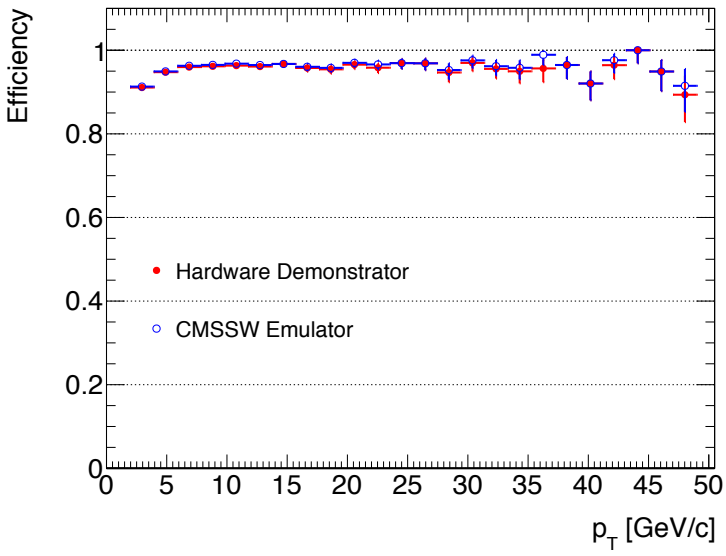

Figure 4.1: Tracking efficiency versus particle transverse momentum obtained with the TMTT hardware demonstrator, when it processes stub data from LHC events taken with 200 pile-up. The results obtained from the demonstrator are compared with those predicted by the software emulation.

2) **In the case of the AM solution** the first demonstrator consisted in two ATCA crates for validating the distribution of the data from the Tracker to the Track Finding Processors. The data from the first crate are grouped in structures long 8 LHC bunch crossing (BX) periods. The receiving boards de-bunch the packets and distribute them to each of the Track Finder boards (the mezzanines) every 500 ns. The setup has demonstrated to be able to perform this time-space data distribution with a latency of 1.2 μs.
The other demonstrator used the two mezzanines (the INFN and FNAL ones). The INFN mezzanine demonstrated the pattern matching efficiency and track reconstruction with state-of-the-art AM06 chips. This is shown in Fig. 2

(left), in which the number of patterns found in the hardware are compared to those expected from the simulation in a sample of ttbar events in 200 PU, full agreement is found. The track reconstruction has also been verified to be in agreement with that expected as shown in Fig. 2 (right). Finally, the FNAL mezzanine was used to measure the latency of the combined pattern matching and track reconstruction stage. The overall latency of the process (from the first stub coming from the detector, to the last track found) is 2.5 μs. In some very dense events, such as those coming from 250 PU, some efficiency is lost for lower pT tracks. These tracks could be recovered by adding additional track fitting modules that increase the latency up to 3.5 μs.

Giacomo Fedi (ER1) has been in charge of qualifying the AM chips, the INFN pattern recognition mezzanine and run the setup.

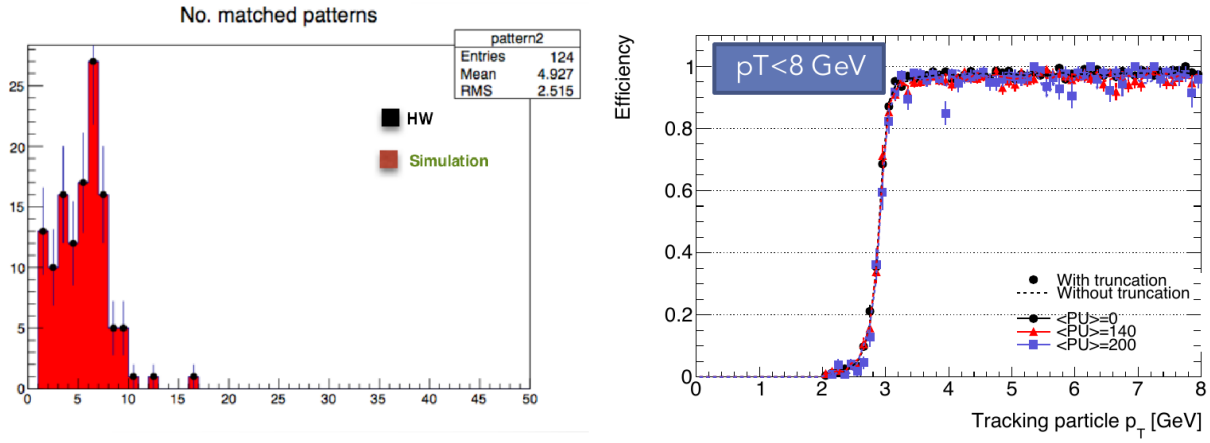

Figure 4.14. Results from the hardware demonstrator. Left: the number of matched patterns per event (ttbar+PU200) in hardware and in simulation. Right: Tracking efficiency funtion of p_T for muons with p_T < 8 GeV

Publications

N.B. Many of the publications listed here were also presented at conferences. Only publications related to the L1 tracking work are listed here, but the INFIERI fellows are also on the author list of numerous other CMS papers.

- G. Fedi, et al. "A pattern recognition mezzanine based on associative memory and FPGA technology for L1 track triggering at HL-LHC", poster presented by G. Fedi at "Frontier Detectors for Frontier Physics", La Biodola (Isola d'Elba, Italy), 24-30 May 2015, published in Nuclear Instruments & Methods in Physics Research A (2015), http://dx.doi.org/10.1016/j.nima.2015.09.086
- G. Fedi et al, "A Pattern Recognition Mezzanine based on Associative Memory and FPGA technology for Level 1 Track Triggers for the HL-LHC upgrade", presented by D. Magalotti at "TWEPP2015", Lisbon (Portugal), 28 Sept. – 2 Oct. 2015, to be published in JINST.
- F. Palla, M. Pesaresi and A. Ryd, "Track Finding in CMS for the Level-1 Trigger at the HL-LHC", presented by M. Pesaresi at "TWEPP2015", Lisbon (Portugal), 28 Sept. – 2 Oct. 2015, **JINST 11 (2016) no.03, C03011,**
- http://dx.doi.org/10.1088/1748-0221/11/03/C03011

- D. Cieri *et al.*, " L1 track finding for a time multiplexed trigger, Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment", ISSN 0168-9002, http://dx.doi.org/10.1016/j.nima.2015.09.117.
- D. Cieri *et al.*, "Hardware Demonstrator of a Level-1 Track Finding Algorithm with FPGAs for the Phase II CMS experiment", proceedings from the ACAT2016 conference, IOP Publishing, Journal of Physics: Conference Series 762 (2016) 012020, doi:10.1088/1742-6596/762/1/012020C.
- **G. Fedi, G. Magazzù, F. Palla.** et al, Track finding based on Associative Memories for Level-1 Triggering in HL-LHC experiments, best paper to the MOCAST 2016 conference, Thessaloniki, Greece, 12-14 May 2016, https://doi.org/10.1109/MOCAST.2016.7495145
- D.Cieri, L.Calligaris *et al.*, "An FPGA-based track finder at Level-1 for the CMS experiment at the High Luminosity LHC", proceedings for the 2016 IEEE Real Time Conference, doi:10.1109/RTC.2016.7543102
- D.Cieri, L.Calligaris *et al.*, "Emulation of a prototype FPGA track finder for the CMS Phase-2 upgrade with the CIDAF emulation framework", proceedings for the 2016 IEEE Real Time Conference, DOI: 10.1109/RTC. 2016.7543110
- D.Cieri, L.Calligaris, L.Ardila-Perez *et al., a comprehensive paper on the FPGA-based track-finding solution is in preparation for publication in JINST.*
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- G. Fedi G., A Pattern Recognition Mezzanine Based on Associative Memory and FPGA Technology for Level-1 Track Triggers for the HL-LHC Upgrade", 2015 IEEE Nuclear Science Symposium and Medical Imaging Conference, San Diego, USA 31Oct-7 Nov, 2015
- G.Fedi ``Associative Memory Pattern Matching for the L1 Track Trigger of CMS at the HL-LHC,'' EPJ Web Conf. 127 (2016) 00008. doi:10.1051/epjconf/201612700008, Connecting the Dots 2016, 22-24 Feb 2016 Vienna (Austria)
- G. Fedi, L1 track trigger for the CMS HL-LHC upgrade using AM chips + FPGA" , CDT/ WIT 2017, Orsay, France 6-9 March, 2017

Talks (not counting those listed under Publications)

All INFIERI fellows on this project have given numerous talks at internal CMS meetings. In addition, they have given the following talks at conferences:

- G. Fedi et al., "A Pattern Recognition Mezzanine based on Associative Memory and FPGA technology for Level-1 Track Triggers for the HL-LHC Upgrade", presented by G. Fedi at "2015 IEEE Nuclear Science Symposium & Medical Imaging Conference", San Diego (USA), 31 Oct. – 7 Nov. 2015.
- G. Fedi, "The L1 Track Finder based on Associative Memories", Talk at the "Vth INFIERI workshop", CERN, Geneva (Switzerland), 27-29 April 2015, https://indico.cern.ch/event/381514/session/6/contribution/13/2/attachments/760406/1043083/infieri.pdf
- 6th INFIERI Workshop, Pisa, Italy 27-29 October, 2015 Talk contribution: "Latest on A.M. based Track Finder" Talk contribution: "Status for A.M. based integration test bench for A.M. based L1 track finder"

- D. Cieri, "The L1 Track Finder based on an all-FPGA's architecture", Talk at the "Vth INFIERI workshop", CERN, Geneva (Switzerland), 27-29 April 2015, https://indico.cern.ch/event/381514/session/6/contribution/13/0/attachments/1132267/1618793/Infieri-workshop.pdf
- D. Cieri, "Track Finding Algorithm for the L1 Track Trigger of the Phase II CMS Experiment", at the IVth INFIERI Workshop – Amsterdam 10-12 December, 2014, https://indico.cern.ch/event/352552/contribution/16/material/slides/4.pdf
- D.Cieri, "L1 Track Finding for a time multiplexed trigger", at the 13th Pisa Meeting on Advanced Detectors, La Biodola, Isola D'Elba, Italy, 24-30 May 2015, https://agenda.infn.it/getFile.py/access?contribId=421&sessionId=17&resId=0&materialId=poster&confId=8397
- D.Cieri, "L1 Track Finding for a time multiplexed trigger", at the Postgraduate days, University of Bristol, Bristol, 15 June 2015
- D.Cieri, "Hardware Demonstrator of a L1 Track Finding Algorithm with FPGAs for the Phase II CMS Experiment", to be presented at the 17th International workshop on Advanced Computing and Analysis Techniques in physics research (ACAT), 18-22 January 2016, Valparaiso, Chile
- L.Calligaris, "Circuit Data Flow (CIDAF): A generic, flexible, discrete-time simulator", 3rd International Summer School on INtelligent Signal Processing for FrontIEr Research and Industry, Hamburg, 14-25 Sept 2015, https://indico.desy.de/conferenceOtherViews.py?view=standard&confId=12535
- L.Calligaris, "Trigger level track reconstruction in CMS with a fully time-multiplexed architecture using a Hough transform implemented in an FPGA", PoS(ICHEP2016)1000
- 7th INFIERI Workshop, Lisbon, Portugal 12-15 April, 2016 Talk contribution: "Progress report on AM at INFN-Pisa""
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- L.Calligaris, "Development of a multi-purpose circuit data flow simulation framework" , 6th INFIERI Workshop, Pisa, 28 Oct 2015, https://indico.cern.ch/event/404880/
- L.Calligaris, "The Track Trigger Proposal, An FPGA-based Level1 track trigger for the Phase-2 CMS Upgrade",
  UK CMS Annual Meeting, 14-15 Jan 2016, Brunel University London

Poster Presentations (not counting those listed under Publications)

- D.Cieri, L.Calligaris "Demonstrator Plans for FPGA-based L1 Track-finding with Hough Transform", at the 3rd International School on Intelligent Signal Processing for Frontier Research & Industry, 14-25 September 2015, Hamburg, Germany, http://infieri-network.eu/sites/default/files/Infieri-poster-hamburg-DCieri.pdf

Outreach

L.Calligaris and D.Cieri both participated in the annual STFC RAL masterclasses on experimental particle physics for hundreds of high school students.

G. Fedi Poster "PhaseII upgrades @CMS" - Researchers' Night, Pisa, Italy, September 25, 2015

G. Fedi Staff member - Bright Pisa - Researchers' Night, Pisa, Italy , September 30, 2016