WP5– Transversal Tool

The aim of this WP is to list all the common tools, available or under development or needed in the network. The network must indeed act as a common platform for sharing these tools and developments and transferring the know-how between the partners and in a cross-community spirit and involving a close contact with Industry. This transfer of knowedge and expertise across-domains is very valuable for the training of the young appointed researchers.

Indeed a series of tools hardware or software based are being developed by all the teams involved in this network in different fields of applications and have been identified as follows:

5.1 Transversal tools for the ASIC design and layout: VDSM and 3D Vertical Interconnect technologies.

The INFIERI project is addressing two main aspects of the Very Deep SubMicron (VDSM) CMOS technology namely the use of 65nm CMOS technology for mix-mode analogue digital Front End ASIC and the 3D technology including 3D vertical interconnect. This is at least the case in HEP.

In INFIERI, the expertise on designing advanced Front End mix-mode ASICs, as for instance for the new FE ASIC for the Phase 2 Pixel detector within the RD53 R&D Collaboration is being developed mainly at CERN, FNAL and INFN. A number of other Labs or Institutions in the network are aiming to get this expertise. Among them there are RAL and NIKHEF. The 65nm CMOS technology expertise has been first developed at CERN in the MEDIPIX collaboration. The Medical team in INFIERI is working on a new design version of this ASIC and thus will be interested to go to 65nm as well (see in subsection 1.3 the NIKHEF section).

Another application of 65nm technology concerns the new Associative Memory device design by INFN and FNAL. Moreover the 65nm will be coupled to the 3D vertical interconnect technology. Such 3D TSV Kit using the Tezzaron technology is available as well. This tool kit will be used for at least two applications in INFIERI, namely: 3D vertical A.M. system by FNAL (VIPRAM) and the WP2-INFIERI demonstrator based on avalanche pixels by CNRS (see Section 2).

Thus the following INFIERI partners are involved or will be involved in using this new CMOS technology, namely: CERN, FNAL, NIKHEF, RAL, CNRS, INFN, Tezzaron. WP5 will help organizing ways to share expertise on using the corresponding toolkits and in exchanging block designs as well as the tools to check and test the designs and layouts (subject indeed of various secondments).

Within the two first INFIERI Summer Schools, dedicated lectures by industrial representatives and also dedicated Lab courses (R. Patti, Tezzaron) are an example of sharing some tools and know-how in the 3D vertical interconnect field. Besides R. Patti (Tezzaron) invited people from MENTOR Graphics design to give lectures at the Schools in Oxford and Paris. These tutorials introduced the audience to the new tools

developed by MENTOR to simulate and test new 3D vertical based layouts. The collaboration with Industry is indeed instrumental in this field.

5.2 Test benches for characterization

Several partners develop a variety of test bench for the characterization of the devices they are developing for the various applications. As an example several Labs in INFIERI have set-up a test bench to characterize and compare SiPM's with MAPMT's. R. White (ULEIC) gave a nice presentation at the Madrid INFIERI workshop[1] where he compares the plethora of test benches for characterizing
SiPMT's in CTA to the first day when Sweden changed driving from UK to EU rules.

The INFIERI workshops allow discussions and exchanges of expertise and trigger exchanged visits between partners. The Madrid workshop for instance was a successful forum where CTA and Medical Imaging partners exchanged experience on SiPM characterization also profiting from the attendance of experts from PHILIPS (Digital SiPM) and V. Saveliev one of the SiPM promoter.

Moreover a series of lectures and Lab courses were given at the Summer Schools in Oxford and Paris. The Lab sessions by V. Saveliev and N. D'Ascenzo using ROOFIT for characterizing SiPMs have proven to be quite useful as well as the ones prepared by CAEN and M. Caccia based on the use of the dedicated kit or the one developed by R.White (ULEIC).

5.3 Development of Fast and Real time algorithms

The development of Fast Real time algorithms is essential both for WP1 and WP4. This is an activity that is being developed in most of the applications in INFIERI, i.e. for the track finder of the L1 outer tracker in CMS (both for the A.M. and for the FPGA based approaches), for the L1 pixel track trigger and for the various real time tasks in SKA as well as in Medical Imaging.

Some techniques developed in one field can prove to be very efficient for other fields, as for instance the growing interest for "sparcity technique"in aAstrophysics, HEP and Medical Imaging.

Lectures were dedicated to this item at the International Summer School in Paris; the INFIERI consortium will further developed the know-how and knowledge transfer in several new software developments for real time algorithm.

[1] Richard White 's presentation aat the INFIERI Workshop in Madrid, January 2014, See https://indico.cern.ch/event/281636/session/19/contribution/43/material/slides/1.pdf

5.4 Test benchmarking platforms to test various accelerators and compare performances

Benchmarking platforms are set up in various places. INFIERI intends coordinating these various test benches. The benchmarking platforms considered here are “generic” platforms, i.e. not dedicated to a specific application and include integration studies. This later case is covered instead by WP6 (see nest section).

Here the idea is to have a generic platform that allows testing various accelerators. Such a platform is for instance set-up at FNAL in the computing division with some partners working on the development of a L1 pixel trigger. It allows benchmarking INTEL Xeon Phi (C++), FPGA’s with VHDL or OPEN-CL, GPGPU with nCUDA or other accelerator under consideration.

The **new ATCA Telecom framework** is becoming the standard in HEP and eventually in SKA or other areas. ESR11 is developing expertise on this item at RAL. WP5 in INFIERI will work on extending the know how across the network. The **µTCA** standard is used for the CMS L1 overall trigger system, the Pixel Signal processing units in Phase 1 and the FPGA based track finder for Phase 2. It will be used for the benchmarking platform for the L1 pixel trigger developments.

Several Labs and Institutions in INFIERI are interested in developing such platforms and sharing knowledge. This is in any case the goal of this project and the young researchers involved in these related tasks are essential to ensure the exchanges across-experiments and communities.

5.5 Simulation tools for feasibility and performances studies

Several simulation tools for feasibility and performances studies have been and are developed in the network in the various fields of applications. Most of the young researchers hired by the network are taking part to it. If these simulation tools are rather experiment-dependent some of the ideas for fast track fitting or imaging can be shared as well as more general and generic fitting or imaging concepts.

The first half of the project was dedicated to develop the specific needed tools for each application. The goal is now to interchange ideas and computing techniques that may prove to be useful in a more interdisciplinary way.