

INtelligent, Fast, Interconnected and Efficient devices, for frontier exploitation in Research and Industry

Funding Scheme: FP7-PEOPLE-2012-ITN

Grant Agreement number: 317446

Project acronym: INFIERI



DELIVERABLE NAME: *New processor based High Performance Computing test bench.*

DELIVERABLE REF. N°: 4.8

WORK PACKAGE: WP4

NATURE OF THE DELIVERABLE: R= Report, P = Prototyped Software, O= Software tools

BENEFICIARY(IES) CONTRIBUTOR(S): TRT THALES

AUTHOR(S) NAME(S) & EMAIL(S): Alberto Garcia Fernandez (ER)

(albertogfernan@gmail.com), Alvin Sashala Naik (ESR)

(alvin.sashalanaik@gmail.com), Philippe Millet (philippe.millet@thalesgroup.com)

Fabrice Lemonnier (fabric.lemonnier@thalesgroup.com), François Duhem

(duhemfrancois@gmail.com)

DELIVERY DATE FROM ANNEX 1: M48

DISSEMINATION LEVEL: RE, CO

PU = Public N/A IN THE INFIERI CONTEXT

PP = Restricted to other programme participants (including the Commission Services) N/A IN THE INFIERI CONTEXT

RE = Restricted to a group specified by the consortium (including the Commission Services) **HIGHLY SUGGESTED IN THE INFIERI CONTEXT**

CO = Confidential, only for members of the consortium (including the Commission Services) **HIGHLY SUGGESTED IN THE INFIERI CONTEXT**

Abstract:

Current high performance computing hardware design involves a first step where chips are benchmarked with functions and computing kernels representative of the core of an algorithm. When such a processor meets the requirements, it is used to build processing boards that will be combined to build processing cabinet for a given application.

Work Description:

Since the benchmark results was effectively representative of the real performance delivered by the system at the end of the development, one could predict the performance of a whole application by combining basic performances figures from the benchmarks.

Project's co-ordinator: Aurore SAVOY NAVARRO

E-mail: aurore@apc.univ-paris7.fr

Period covered: from 01/02/2013 to 31/01/2017

Project website: <http://infieri-network.eu>

INtelligent, Fast, Interconnected and Efficient devices, for frontier exploitation in Research and Industry

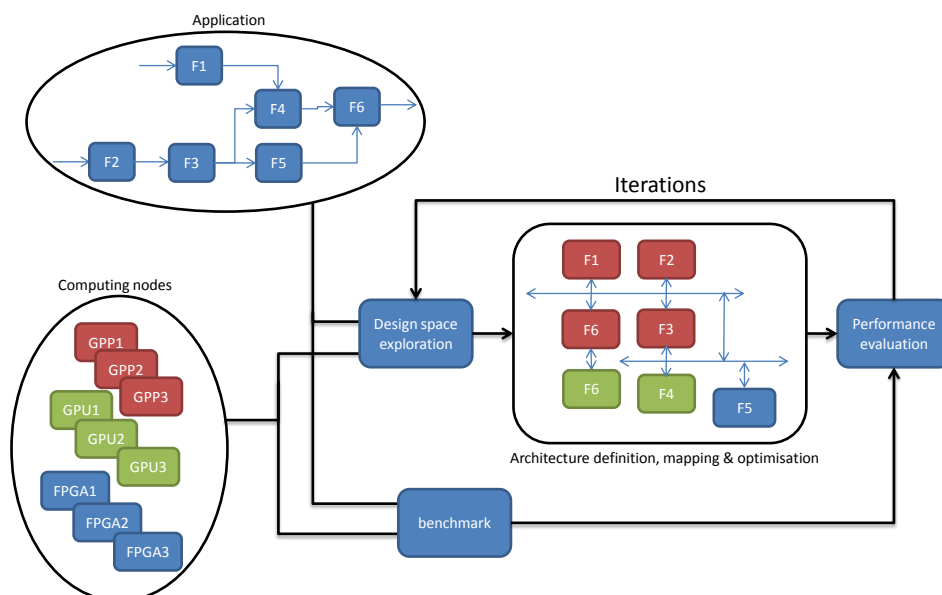
Funding Scheme: FP7-PEOPLE-2012-ITN

Grant Agreement number: 317446

Project acronym: INFIERI



With the increase of the complexity of the processors – number of cores, parallelism, heterogeneity – and the increase complexity of the memory hierarchy and memory access (e.g. through NoCs), it becomes very tricky, when not impossible, to predict performances of a whole application only given a few unary benchmarks on the targeted chip.



In order to improve the design process of high performance computing hardware, we need to assist the hardware designer with tools that can predict rough performances of an application on a given chip or on a given combination of chips. Moreover, the number of possible computing nodes is more and more important and it becomes impossible for the designer of the platform to explore efficiently the space of solutions. Therefore it is necessary to provide some tools to automatize the exploration of the design space of solutions.

The work consisted in

Define the needs.

Understand what is available today and what is the gap between the capabilities of these tools and our needs.

Define orientation and research tracks to develop further such tools and ease the design space exploration.

Talks:

INtelligent, Fast, Interconnected and Efficient devices, for frontier exploitation in Research and Industry

Funding Scheme: FP7-PEOPLE-2012-ITN

Grant Agreement number: 317446

Project acronym: INFIERI



Alvin Sashala Naik, APC Lab, CNRS (ESR1.2), *“Fast Iteration on prototyping in HPC medical applications: a case study with Mentor Vista”*, 8th INFIERI Workshop, held at FNAL, Batavia (USA), October 17-21, 2016

Alberto Garcia, THALES-TRT (ER5), *“Efficient Prototyping in High Performance Computing for Medical Applications”*, 8th INFIERI Workshop, held at FNAL, Batavia (USA), October 17-21, 2016

Francois Duhem, THALES-TRT, *“Research Objectives of Thales Research & Technology in embedded HPC and MPC domains”*, 8th INFIERI Workshop, held at FNAL, Batavia (USA), October 17-21, 2016

All these 3 presentations are in the Website of the 8th INFIERI workshop at FNAL:

<https://indico.cern.ch/event/557734/overview>

Poster Presentations

Poster by Alvin Sashala Naik (CNRS) at the 8th Workshop at FNAL, Batavia, October 17-21, 2016.

Poster by Alberto Garcia (TRT) at the 8th Workshop at FNAL, Batavia, October 17-21, 2016.

Poster by Alberto Garcia (TRT) at the 4th International Summer School at University of Sao Paulo, USP, (Brazil), 23/1-3/2, 2017, See poster session in the School website:

<http://www.usp.br/ime/infieri2016>

Youtubes: Two Youtubes by Alvin Sashala Naik and by Alberto Garcia on the INFIERI network website:

<http://infieri-network.eu>, Click on “Youtubes”

Outreach event:

Alvin Sashala Naik (CNRS), Poster presentation at the “Journée Scientifique: Le Numérique, Parlons en!” held at the Université Paris Diderot, December 8, 2016,

See “News and events” in the frontpage of the INFIERI website: <http://infieri-network.eu>

Project’s co-ordinator: Aurore SAVOY NAVARRO

E-mail: aurore@apc.univ-paris7.fr

Period covered: from 01/02/2013 to 31/01/2017

Project website: <http://infieri-network.eu>