INtelligent, Fast, Interconnected and Efficient devices, for frontier exploitation in Research and Industry

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Grant Agreement number: 317446

Project acronym: INFIERI

DELIVERABLE NAME: ***Design of a Novel Level-1 (real-time) Pixel Trigger Prototype for the High Luminosity LHC experiments: prototype evaluation and results***

DELIVERABLE REF. N°: 1.3/1.4

WORK PACKAGE: WP1

NATURE OF THE DELIVERABLE: ☒ **R**= Report, **X P** = Prototype

BENEFICIARY(IES) CONTRIBUTOR(S): CNRS (APC), FNAL, INFN

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DELIVERY DATE FROM ANNEX 1: M48

DISSEMINATION LEVEL: ☐**RE**, ☒**CO**

PU = Public N/A IN THE INFIERI CONTEXT
PP = Restricted to other programme participants (including the Commission Services) N/A IN THE INFIERI CONTEXT
RE = Restricted to a group specified by the consortium (including the Commission Services) **HIGHLY SUGGESTED IN THE INFIERI CONTEXT**
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Abstract: The aim is to prototype a novel real-time selection (Level-1 trigger) based on the pixel detectors at LHC experiment for the upgrade at high luminosity of the machine (expected by 2025). The Physics potential and performances are summarized in (WP1.1), the design features are in (WP1.2). The WP1.3 deliverable focuses on the prototype evaluation and WP1.4 on related results.

Work description:

The main constraints are the bandwidth and latency to be confronted with one Giga pixels in total in this new device, and a total Level-1 latency of about 10 microseconds. The main way of overcoming these two challenging issues is by ***seeding the pixel track pattern recognition*** with external fast detectors that define in a very few microseconds the ***regions of interest (RoI)***. The RoI are the regions where to look for the relevant pixel detector region (bandwidth reduction). The other step is developing ultra-fast real-time algorithms together with using advanced FEE and processor technology. To achieve these goals INFIERI led an activity looking how this can be achieved in real life.

This leads to have a signal and data processing architecture that includes:

- ✓ Zero suppression (sparcification)
- ✓ Data compression

- ✓ Pixel hits clusterization
- ✓ Seeded Level 1 trigger (based on Region of Interest, RoI)
- ✓ Rate capability

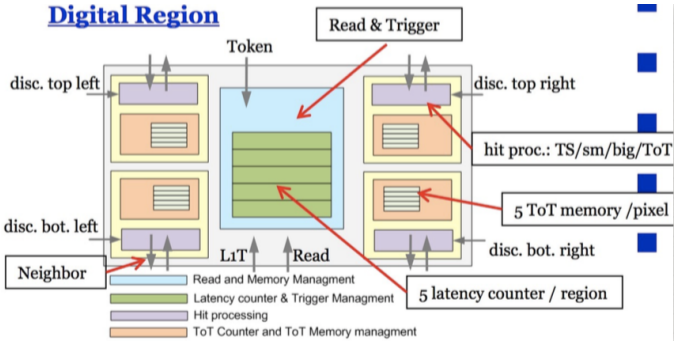
The studies carried on over the last year of the project concluded that all these above points can be included in the FEE and readout architecture of the Front-End Readout ASIC. Based on the participation to the RD53 Very Front End (VFE) ASIC design (ESR1.1 at CNRS, FNAL, INFN) the two first points are addressed. A compressor possibly included in the VFE ASIC gives a compression factor of 2.

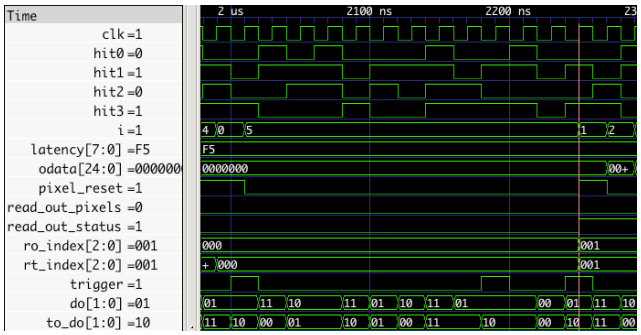
The next important step addressed the three last points here below. Among pre-existing architectures the FEI4b [Fig 1] developed by ATLAS is chosen as the best "playground" for further developing these 3 points. It is preferred to a studied alternative based on adding CAM's [Fig 2] in the signal/data processing architecture.

This architecture includes: ***sparcification; clusterization; a second L1 trigger capability*** (indeed by adding latency counters); ***distributed latency counter and hit storage*** in the pixel array, not the end of column logic, thus maintaining high efficiency at very high rate.

The VERILOG modeling of this new architecture is achieved [Fig3] and leads to very encouraging results on the realistic feasibility of this ***first pattern recognition stage*** in the FE hardware architecture.

The next step deals with the data processing step, i.e. ***the pattern recognition and track reconstruction.*** Two alternatives are considered: one based on the new MICRON automata processor. A complete study, both software and hardware, is achieved by FNAL, MICRON and CNRS (Fig4). It uses the PiXTrK algorithm in real time mode for the pattern recognition. The results indicate that the present MICRON processor prototype cannot achieve the requested performances in latency. The alternative is the L1 track finder for the outer tracker. The performances achieved (WP4.6) show that a latency of ~3 µs looks feasible.





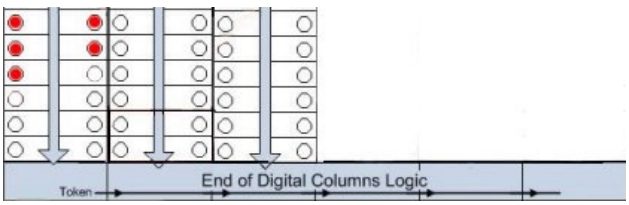


Fig. 1: Top Left shows the schematics of the FEI4b signal processing for the region clustering 4 pixels and eventually neigbhours. Fig 3: right top shows the VERILOG modeling of a cluster and pixel schema below.

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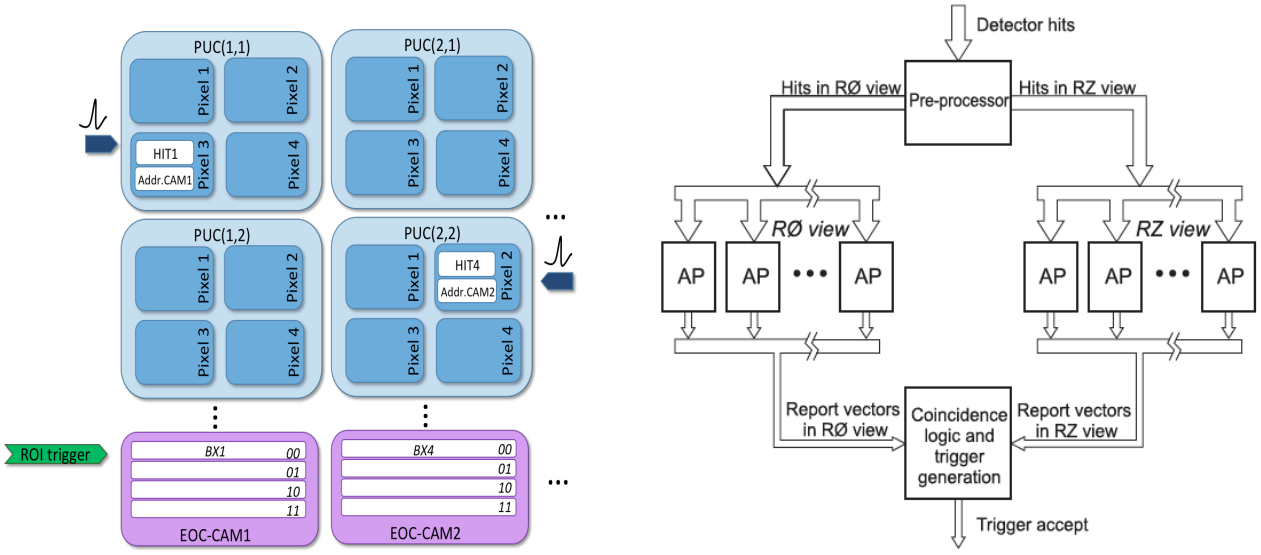

Left: Schema of readout architecture including End of Column CAM's (Fig2); Right: Block diagram of the automata Processor Implementation of the PiXtrK algorithm in the MICRON processor prototype.

Publications

[1] C.S. Moon and A. Savoy Navarro, "Level-1 pixel based tracking trigger algorithm for LHC upgrade", Journal of Instrumentation, JINST 10 (2015).

[2] M.Wang, G. Cancelo, C. Green, D. Guo, K.Wang, T. Zmuda, "Fast Track Pattern Recognition in High Energy Physics Experiments with the Micron Automata Processor", FERMILAB-PUB-16-013-CD (2016) and NIMA 832, 2016, 219-230. And several other presentations at International conferences.

[3] References quoted for the L1 track finder in WP4.6.

Talks by ESRs

"Development of a data compressor for the CMS phase II pixel detector", INFIERI, 5th, 6th and 7th Workshop, by S. Poulios and K. Androsov.

Poster Presentations

[1] "*Online Data Reduction and Local Digital Clustering*", INFIERI 4th Workshop & Mid-Term Review, 10-12 December 2014, NIKHEF, Amsterdam by S. Poulios.

https://indico.cern.ch/event/352552/contribution/16/material/slides/12.png

[2] "Development of a data compressor for the CMS phase II pixel detector", 3rd International Summer School on INtelligent Signal Processing for FrontIEr, Research and Industry, 14-25 September 2015, Hamburg, Germany by S. Poulios.

https://indico.desy.de/getFile.py/access?contribId=67&sessionId=17&resId=0&materialId=slides&confId=12535

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Period covered: from 01/02/2013 to 31/01/2017
Project website: http://infieri-network.eu

[3] A. Bogachev and S. Lapin, "*Verilog Modeling of a RoI Fast Level1 Pixel Track Trigger Strategy for LHC*" at the International Summer School INFIERI, University of Sao Paulo, USP, January 23-Feb 4, 2017.
https://www.usp.br/ime/infieri2016

Several PhD Theses including these topics: B. Nodari (ESR1.1 fellow at CNRS), S. Poulios (ESR6 fellow at INFN-Pisa), A. Bogachev (ESR1.4 fellow at CNRS), S. Lapin (ESR1.5 fellow at CNRS).