INtelligent, **F**ast, **I**nterconnected and **E**fficient devices, for frontier exploitation in **R**esearch and **I**ndustry

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DELIVERABLE NAME: Design of a Novel Level-1 (real-time) Pixel Trigger Prototype for the High Luminosity LHC experiments

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WORK PACKAGE: WP1

NATURE OF THE DELIVERABLE: ☒ **R**= Report, **X P** = Prototype,

BENEFICIARY(IES) CONTRIBUTOR(S): CNRS (APC), FNAL, INFN, LIP, SNU

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DISSEMINATION LEVEL: ☐**RE**, ☒**CO**

PU = Public N/A IN THE INFIERI CONTEXT
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Abstract: The aim is to develop and prototype a novel real-time selection (Level-1 trigger) based on the pixel detectors at LHC experiment for the upgrade at high luminosity of the machine (expected by 2025). The Physics potential and feasibility of such a challenging system has been studied in depth these past 3 years (WP1.1). In 2015 the design of this trigger system has been developed (WP1.2).

Work description:

The main constraints are the bandwidth and latency to be confronted taking into account that there will a one Giga pixels in total in this new device, and that the total Level1 latency will be about 10 microseconds. The main features for overcoming these two very challenging issues is by seeding the track pattern recognition with external fast detectors that allow to define very quickly the regions of interest where to look the interesting pixel detector region (bandwidth reduction) and developing ultra-fast real-time algorithm together with using advanced processor technology. Therefore the design we have developed for this trigger includes:

1) Developing new features in the design/layout of the novel Front End ASIC (ESR1.1) that process the signal from the pixels with data compression, experiencing two encoding methods (Hoffmann and Arithmetic one) included in VHDL in the FE architecture design (ESR6) (see WP1.3/WP1.4).
2) Or hardware and firmware implementation of hits clusterisation in this ASIC (see WP1.3).
3) The development of one benchmarking platform option to test and further develop the overall design, this goes beyond deliverable WP1.2 and the INFIERI project goals but has been already implemented in 2015 on a new Automata Processor from MICRON where the real-time algorithm developed in WP4 (PiXTRK) has been implemented.

A complete design is presented in the CMS Internal Detector Note, CMS-DN 15-008, "A Level-1 pixel based track trigger for CMS upgrade" signed by all involved ESR's and 2 publications in Journals (Figs 1 and 2)

Publications

[1] C.S. Moon and A. Savoy Navarro, "Level-1 pixel based tracking trigger algorithm for LHC upgrade", Journal of Instrumentation, JINST 10 (2015).

[2] M.Wang, G. Cancelo, C. Green, D. Guo, K.Wang, T. Zmuda, "Fast Track Pattern Recognition in High Energy Physics Experiments with the Micron Automata Processor", FERMILAB-PUB-16-013-CD (2016), submitted to NIMA.

Talks by ESRs

[1] "First look at data compression", RD53 Meeting, 24 April, CERN, Geneva
https://indico.cern.ch/event/378099/session/7/contribution/38/material/slides/0.pdf

[2] "Compactification of pixel data at the FEE", INFIERI 5th Workshop, 27-29 April 2015, CERN, Geneva
https://indico.cern.ch/event/381514/session/7/contribution/31/material/slides/1.pdf

[3] "First look at data compression", CMS Tracker Phase II days, 21 May 2015, CERN, Geneva
https://indico.cern.ch/event/392299/contribution/11/material/slides/1.pdf

[4] "Development of a data compressor for the CMS phase II pixel detector", INFIERI 6th Workshop, 27-29 October 2015, INFN Pisa, Italy

Poster Presentations

[1] "Online Data Reduction and Local Digital Clustering", INFIERI 4th Workshop & Mid-Term Review, 10-12 December 2014, NIKHEF, Amsterdam.

https://indico.cern.ch/event/352552/contribution/16/material/slides/12.png

[2] "Development of a data compressor for the CMS phase II pixel detector", 3rd International Summer School on INtelligent Signal Processing for FrontIEr Research and Inustry, 14-25 September 2015, Hamburg, Germany. https://indico.desy.de/getFile.py/access?contribId=67&sessionId=17&resId=0&materialId=slides&confId=12535

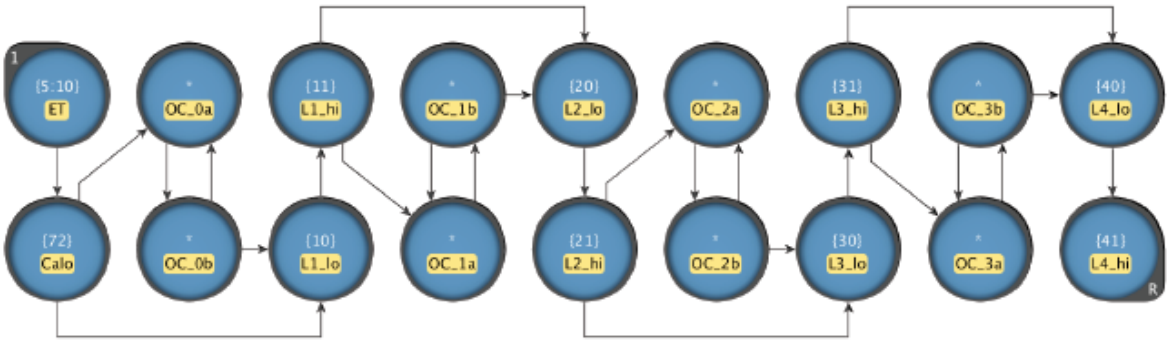
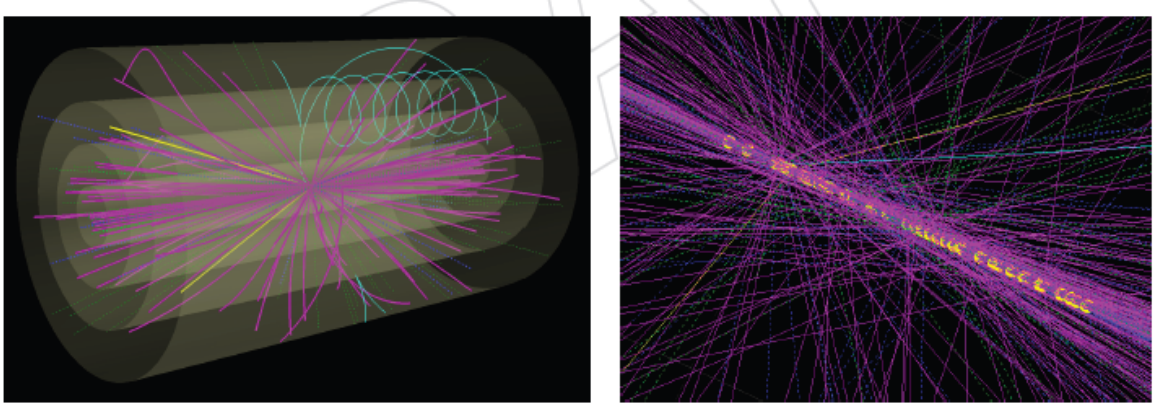


Fig 1. An Automata network programmed to generate a report on matching a specific sequence of exactly 4 pixel hit addresses



(a) (b)

Fig 2. Views of an event as simulated in a) of the overall pixel detector and b) with a zoom extremely close to the beam pipe where occurs the collision that produces the event. This is where the pattern recognition with this automata processor is experienced on the benchmarking platform.