

INtelligent, **F**ast, **I**nterconnected and **E**fficient devices, for frontier exploitation in **R**esearch and **I**ndustry

Funding Scheme: FP7-PEOPLE-2012-ITN

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Project acronym: INFIERI



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NATURE OF THE DELIVERABLE: R= Report

BENEFICIARY(IES) CONTRIBUTOR(S): INFN, CERN, FNAL, STFC (=RAL/UBRIS)

AUTHOR(S) NAME(S) & EMAIL(S):

Giacomo Fedi (ER1), Giacomo.Fedi@pi.infn.it

Fabrizio Palla, Fabrizio.Palla@pi.infn.it

Duccio Abbaneo, Duccio.Abbaneo@cern.ch

Ian Tomalin, ian.tomalin@stfc.ac.uk

Claire Shepherd-Themistocleous, Claire.Shepherd-Themistocleous@cern.ch

Dave Newbold, Dave.Newbold@cern.ch

Davide Cieri (ESR11), Davide.Cieri@stfc.ac.uk

Luigi Calligaris (ER2), Luigi.Calligaris@stfc.ac.uk

Luis Ardila-Perez (ESR11.2), Luis.Ardila@kit.edu

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DISSEMINATION LEVEL: RE, CO

PU = Public **N/A IN THE INFIERI CONTEXT**

PP = Restricted to other programme participants (including the Commission Services) **N/A IN THE INFIERI CONTEXT**

RE = Restricted to a group specified by the consortium (including the Commission Services) **HIGHLY SUGGESTED IN THE INFIERI CONTEXT**

CO = Confidential, only for members of the consortium (including the Commission Services) **HIGHLY SUGGESTED IN THE INFIERI CONTEXT**

Abstract

The design of the CMS Silicon Outer Tracker upgrade for HL-LHC has been developed in a collaborative effort led by the CERN Associated Partner with other CMS groups and is sketched in Fig. 1. D. Abbaneo presented the work at the 5th INFIERI workshop. A key aspect of the design is to facilitate off-detector reconstruction of the trajectories of charged particle tracks with transverse

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momentum (p_T) above a few GeV/c, and doing so sufficiently quickly that these tracks could be used for the L1 trigger decision.

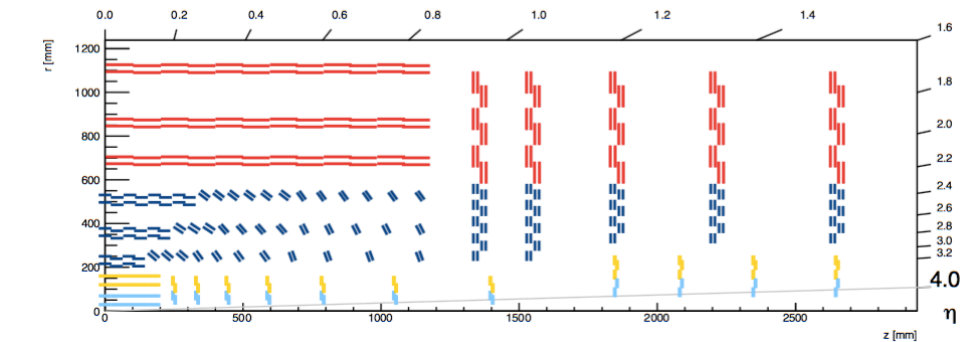


Figure 1: A quarter of the CMS Upgrade Tracker layout. The blue and red lines correspond to the p_T -modules for the Outer Tracker. The yellow and light blue lines are the Inner pixel detector.

The CERN Associated partner contributed to the design of the so-called p_T -modules: these are made of two closely spaced (a few mm) silicon sensors, both read out by the same electronics. Particles traversing these modules produce a pair of clusters (known as a “stub”), which is retained if it is compatible with a particle of p_T exceeding about 2 GeV/c. This threshold reduces the data rate of stubs that must be transmitted to the off-detector track-reconstruction hardware by an order of magnitude. There are two types of modules: those at large radii, made of two silicon strip sensor, and those closer to the beam composed of a silicon strip sensor and a macro-pixel sensor. CERN is developing a small prototype for the innermost layers, readout by the same electronics. Its features are sketched in Fig. 2.

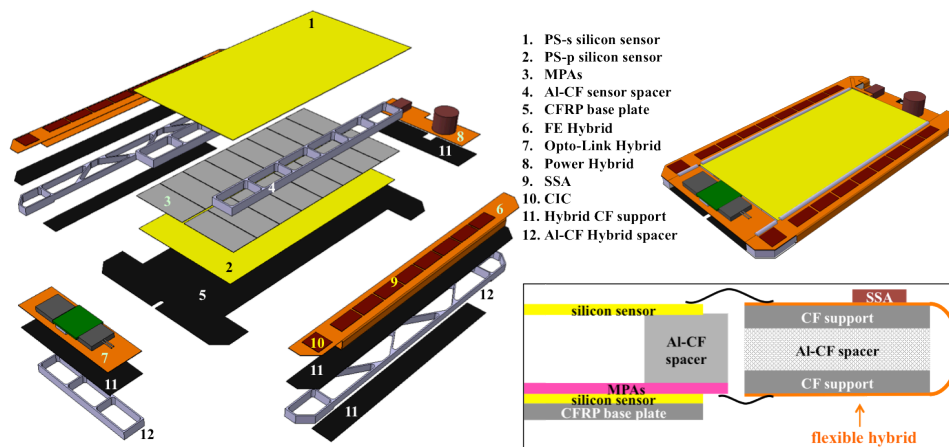


Figure 2. Exploded view of the Pixel + strip p_T -module components (left), 3D view of the assembled module (upper right), and a sketch of the Front-End electronics.



These hit-pairs (stubs) are then transferred to some electronic boards (sitting off-detector) that perform track reconstruction, using the information of all layers. Within the context of INFIERI, two alternative proposals exist for this electronics. One uses custom ‘associative memory’ (AM) chips in combination with FPGAs, developed mainly by the INFN and FNAL communities together with non-INFIERI partners, such as Lyon, KIT and some US, Brazilian and Indian Universities, and the other, named “TMTT” (Time Multiplexed Track Trigger), uses only FPGAs and is developed by STFC, CERN (INFIERI partners) and other non-INFIERI collaborators, i.e. KIT and Vienna. Several EU INFIERI fellows both from INFN (Giacomo Fedi (ER1)) and from STFC at RAL and Bristol (Davide Cieri (ESR11.1), Luigi Calligaris (ER2) and Luis Ardilla Lopes (ESR11.2)) were involved in this work.

In the AM solution, efforts were concentrated on performing pattern recognition using a chip originally developed by INFN, based on the concept of Associative Memory (AM). The AM chip contains large numbers of “patterns”, each corresponding to a possible particle trajectory. It is able to test the consistency of each input stub with each of these patterns in parallel, providing very rapid track-finding. Stubs that the AM identifies as being consistent with a track candidate are then processed in an FPGA that cleans that tracks and then fits a helix to them using the Principal Component Analysis technique. The performance of the track fit is excellent, as illustrated by the efficiency plot in Fig. 3 (left).

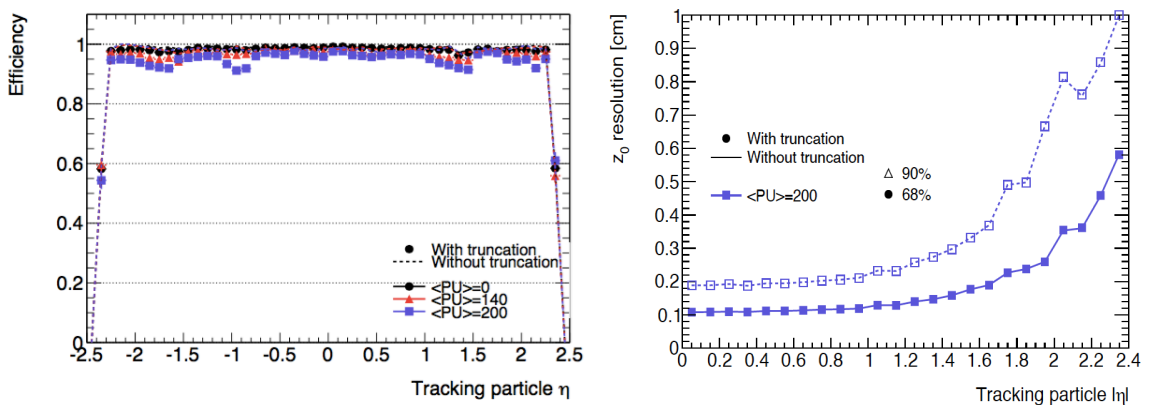


Figure 3. Performance of the L1 track-reconstruction algorithms. The left plot shows the efficiency of the AM-based solution to reconstruct muons of $p_T > 8$ GeV in $t\text{-}\bar{t}$ +pileup events as a function of pseudorapidity. The right-plot shows for the TMTT solution, the resolution in longitudinal impact parameter as a function of pseudorapidity when reconstructing tracks in high Pt jets within simulated $t\text{-}\bar{t}$ events taken with 200 pileup.

In the case of the TMTT proposal, the concept could be demonstrated using pre-existing high-speed data processing cards, known as MP7, each equipped with a Xilinx Virtex7 FPGA, with cards communicating with each other via optical links with a total bandwidth of ~ 1 Tb/s. Effort could

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therefore be focused on the track reconstruction algorithm development, its implementation in firmware, and a study of its performance on the hardware demonstrator. Fig. 3 (right) shows the typical performance of the chosen tracking algorithm, which satisfies CMS requirements.

Publications

N.B. Many of the publications listed here were also presented at conferences. Only publications related to the L1 tracking work are listed here, but the INFIERI fellows are also on the author list of numerous other CMS papers.

- G. Fedi, et al. “A pattern recognition mezzanine based on associative memory and FPGA technology for L1 track triggering at HL-LHC”, poster presented by G. Fedi at “Frontier Detectors for Frontier Physics”, La Biodola (Isola d’Elba, Italy), 24-30 May 2015, published in Nuclear Instruments & Methods in Physics Research A (2015), <http://dx.doi.org/10.1016/j.nima.2015.09.086>
- G. Fedi et al, “A Pattern Recognition Mezzanine based on Associative Memory and FPGA technology for Level 1 Track Triggers for the HL-LHC upgrade”, presented by D. Magalotti at “TWEPP2015”, Lisbon (Portugal), 28 Sept. – 2 Oct. 2015, to be published in JINST.
- F. Palla, M. Pesaresi and A. Ryd, “Track Finding in CMS for the Level-1 Trigger at the HL-LHC”, presented by M. Pesaresi at “TWEPP2015”, Lisbon (Portugal), 28 Sept. – 2 Oct. 2015, **JINST 11 (2016) no.03, C03011**, <http://dx.doi.org/10.1088/1748-0221/11/03/C03011>
- D. Cieri *et al.*, “L1 track finding for a time multiplexed trigger, Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment”, ISSN 0168-9002, <http://dx.doi.org/10.1016/j.nima.2015.09.117>.
- D. Cieri *et al.*, “Hardware Demonstrator of a Level-1 Track Finding Algorithm with FPGAs for the Phase II CMS experiment”, proceedings from the ACAT2016 conference, IOP Publishing, Journal of Physics: Conference Series 762 (2016) 012020, doi:10.1088/1742-6596/762/1/012020C.
- **G. Fedi, G. Magazzù, F. Palla.** et al, [Track finding based on Associative Memories for Level-1 Triggering in HL-LHC experiments](https://doi.org/10.1109/MOCAST.2016.7495145), best paper to the MOCAST 2016 conference, Thessaloniki, Greece, 12-14 May 2016, <https://doi.org/10.1109/MOCAST.2016.7495145>
- D.Cieri, L.Calligaris *et al.*, “An FPGA-based track finder at Level-1 for the CMS experiment at the High Luminosity LHC”, proceedings for the 2016 IEEE Real Time Conference, doi:10.1109/RTC.2016.7543102
- D.Cieri, L.Calligaris *et al.*, “Emulation of a prototype FPGA track finder for the CMS Phase-2 upgrade with the CIDAF emulation framework”, proceedings for the 2016 IEEE Real Time Conference, DOI: 10.1109/RTC.2016.7543110
- D.Cieri, L.Calligaris, L.Ardila-Perez *et al.*, *a comprehensive paper on the FPGA-based track-finding solution is in preparation for publication in JINST.*
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Project’s co-ordinator: Aurore SAVOY NAVARRO

E-mail: aurore@apc.univ-paris7.fr

Period covered: from 01/02/2013 to 31/01/2017

Project website: <http://infieri-network.eu>

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- G. Fedi G., "A Pattern Recognition Mezzanine Based on Associative Memory and FPGA Technology for Level-1 Track Triggers for the HL-LHC Upgrade", 2015 IEEE Nuclear Science Symposium and Medical Imaging Conference, San Diego, USA 31 Oct-7 Nov, 2015
- G. Fedi "Associative Memory Pattern Matching for the L1 Track Trigger of CMS at the HL-LHC," EPJ Web Conf. 127 (2016) 00008. doi:10.1051/epjconf/201612700008, Connecting the Dots 2016, 22-24 Feb 2016 Vienna (Austria)
- G. Fedi, "L1 track trigger for the CMS HL-LHC upgrade using AM chips + FPGA", CDT/ WIT 2017, Orsay, France 6-9 March, 2017
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Talks (not counting those listed under Publications)

All INFIERI fellows on this project have given numerous talks at internal CMS meetings. In addition, they have given the following talks at conferences:

- G. Fedi et al., "A Pattern Recognition Mezzanine based on Associative Memory and FPGA technology for Level-1 Track Triggers for the HL-LHC Upgrade", presented by G. Fedi at "2015 IEEE Nuclear Science Symposium & Medical Imaging Conference", San Diego (USA), 31 Oct. – 7 Nov. 2015.
- G. Fedi, "The L1 Track Finder based on Associative Memories", Talk at the "Vth INFIERI workshop", CERN, Geneva (Switzerland), 27-29 April 2015, <https://indico.cern.ch/event/381514/session/6/contribution/13/2/attachments/760406/1043083/inferi.pdf>
- 6th INFIERI Workshop, Pisa, Italy 27-29 October, 2015 Talk contribution: "Latest on A.M. based Track Finder" Talk contribution: "Status for A.M. based integration test bench for A.M. based L1 track finder"
- D. Cieri, "The L1 Track Finder based on an all-FPGA's architecture", Talk at the "Vth INFIERI workshop", CERN, Geneva (Switzerland), 27-29 April 2015, <https://indico.cern.ch/event/381514/session/6/contribution/13/0/attachments/1132267/1618793/Inferi-workshop.pdf>
- D. Cieri, "Track Finding Algorithm for the L1 Track Trigger of the Phase II CMS Experiment", at the IVth INFIERI Workshop – Amsterdam 10-12 December, 2014, <https://indico.cern.ch/event/352552/contribution/16/material/slides/4.pdf>
- D. Cieri, "L1 Track Finding for a time multiplexed trigger", at the 13th Pisa Meeting on Advanced Detectors, La Biodola, Isola D'Elba, Italy, 24-30 May 2015, <https://agenda.infn.it/getFile.py/access?contribId=421&sessionId=17&resId=0&materialId=poster&confId=8397>
- D. Cieri, "L1 Track Finding for a time multiplexed trigger", at the Postgraduate days, University of Bristol, Bristol, 15 June 2015
- D. Cieri, "Hardware Demonstrator of a L1 Track Finding Algorithm with FPGAs for the Phase II CMS Experiment", to be presented at the 17th International workshop on Advanced Computing and Analysis Techniques in physics research (ACAT), 18-22 January 2016, Valparaiso, Chile

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- L.Calligaris, "Circuit Data Flow (CIDAF): A generic, flexible, discrete-time simulator", 3rd International Summer School on INtelligent Signal Processing for FrontIer Research and Industry, Hamburg, 14-25 Sept 2015, <https://indico.desy.de/conferenceOtherViews.py?view=standard&confId=12535>
- L.Calligaris, "Trigger level track reconstruction in CMS with a fully time-multiplexed architecture using a Hough transform implemented in an FPGA", PoS(ICHEP2016)1000
- 7th INFIERI Workshop, Lisbon, Portugal 12-15 April, 2016 Talk contribution: "Progress report on AM at INFN-Pisa"
-
- L.Calligaris, "Development of a multi-purpose circuit data flow simulation framework", 6th INFIERI Workshop, Pisa, 28 Oct 2015, <https://indico.cern.ch/event/404880/>
- L.Calligaris, "The Track Trigger Proposal, An FPGA-based Level1 track trigger for the Phase-2 CMS Upgrade", UK CMS Annual Meeting, 14-15 Jan 2016, Brunel University London

Poster Presentations (not counting those listed under Publications)

- D.Cieri, L.Calligaris "Demonstrator Plans for FPGA-based L1 Track-finding with Hough Transform", at the 3rd International School on Intelligent Signal Processing for Frontier Research & Industry, 14-25 September 2015, Hamburg, Germany, <http://infiere-network.eu/sites/default/files/Infiere-poster-hamburg-DCieri.pdf>

Outreach

L.Calligaris and D.Cieri both participated in the annual STFC RAL masterclasses on experimental particle physics for hundreds of high school students.

G. Fedi Poster "PhaseII upgrades @CMS" - Researchers' Night, Pisa, Italy, September 25, 2015

G. Fedi Staff member - Bright Pisa - Researchers' Night, Pisa, Italy, September 30, 2016